Title: Digital Design Engineer – Autonomous Driving SOC (Entry Level)

FABU America Inc. **Contact: min.dang@fabu.ai**

The future is bright for autonomous driving (AD) with the rapid technology advances in artificial intelligence, machine learning, computer vision, sensor fusion, and silicon technology. Join us to be at the forefront of this incredible journey!

FABU America Inc. was founded in early 2018 with strong financial backing from world-renowned investors. The company has offices in Tempe, AZ, San Diego, CA, and Hangzhou, China. We develop intelligent System-on-Chips (SoCs) for autonomous driving. Our proprietary deep learning algorithms and custom acceleration architecture will revolutionize in-vehicle information processing and enable L3-L5 autonomous driving and advanced driver-assistance systems (ADAS).

We are seeking qualified candidates to fill multiple SoC Engineering positions in our San Diego Design Center. You will work with a world-class engineering team to develop the next-generation SoC for autonomous driving.

Job Duties:

- Understanding the Arch/design/Verification requirements thoroughly
- Perform Verilog RTL coding of block level designs.
- Coordinate with other designers and perform SoC level integration of design blocks.
- Qualify RTL code with frontend design tools such as Lint & CDC.
- Verify synthesis results using LEC tools.
- Work closely with Design Verification team in helping fix design bugs and in achieving code coverage and functional coverage closure.
- Test case and test bench components coding
- Run pre-Si power estimation tools prior to tape out.
- Regression & Debugging

Perks:

- Medical, Vision, and Dental benefits
- Company 401(K) program
- Work with world-class engineers
- Shape the future of the autonomous driving industry

Location: San Diego.

Qualifications:

- Familiarity with ASIC/SoC design flows and methodologies
- Familiarity with Verilog/System Verilog, Perl, Python.
- Understanding of logic synthesis and digital design.
- Knowledge of computer architecture concepts.
- Knowledge of fixed-point arithmetic concepts.
- Experience with industry-standard EDA tools: Synthesis and/or Static timing analysis, LEC, Linting.
- Ability to be a self-starter in a dynamic environment with rapidly changing requirements.
- Highly motivated, obsession with delivery quality and customer-oriented
- Prior internship in ASIC/SoC related work is a plus

Education Requirements Required: Bachelor's, Electrical Engineering, Science, or related fields
Preferred: Master's, Electrical Engineering

Keywords Linting, Spyglass, Verilog, System Verilog, Power Artist, DFT, DFD, Design-for-Test, Design-for-Debug, MBIST, ATPG, Scan, ATPG tools, RTL, verification, SOC, UVM, ASIC, SoC