Talent Profile-
Wireless HW Design & DV
Wireless HW Digital Design/Verification
(Talent Profiles)

Minimum Qualifications
• Programming in Python, C, Perl, Verilog, SystemVerilog, Matlab, Shell, Tcl
• Computer Architecture, Digital Design, VLSI Design, ASIC
• RTL, Verification (OVM, UVM), Lab debug, Physical Design
• Formal techniques, High Level Synthesis

Technical Track
- Architecture
- Design
- Validation
- Implementation

Additional Qualifications
• Digital signal processing
• Wireless communication, communication theory
• Standards : Cellular (LTE, 5G) and WiFi (802.11 be), etc
• Algorithms, Modelling, Timeline

• Digital Design, Microarchitecture
• Datapath, control processors, Infrastructure
• Low Power

• Digital Verification - Testbenches, test plans, Checkers
• Formal verification, Coverage closure
• Bit exact matching with models, control path verification
• Lab debug, Emulation

• Synthesis and Timing constraints
• Design for Test (DFT, MBIST)
• Place-and-Route, Timing Closure

Bachelors/Masters/Ph.D.: Electrical Engineering, Computer Engineering, Electrical & Computer Engineering

Volume: High
Niche Skillset Level: Medium
Interested in a HW Design/ Design Verification Internship?

Please Apply here:

[HW Digital Design & DV Internship- Summer 2023](#)

REQ #3042988