# FREQUENCY MULTIPLICATION WITH HIGH-POWER MICROWAVE FIELD-EFFECT TRANSISTORS*

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## ABSTRACT

The experimentally measured characteristics of a 4-to-8 GHz FET frequency doubler are described. A non-linear circuit model for microwave FETs is proposed and is shown useful for predicting and optimizing the doubler performance, and for calculating the design parameters.

## Introduction

Field-effect transistors, and in particular the GaAs MESFETs presently available for use at microwave frequencies, are inherently nonlinear devices. As a result, they have been used not only for linear applications (like amplification) but also several nonlinear applications, including frequency conversion, power limiting, modulation, and high-speed logic. Recently, some authors have qualitatively discussed their use as frequency multipliers and have reported some preliminary experimental results.[1-2] This paper describes a detailed quantitative study of harmonic generation in microwave FET circuits. The successive sections of the paper describe (a) the experimental measurement of the performance of a 4 GHz-to-8 GHz frequency doubler, constructed with a FET device which has been separately characterized in detail, (b) the identification of those nonlinearities of the device which are significant in the present application and the development of a nonlinear circuit model of FET, and (c) a calculation of the expected performance of the frequency doubler and its comparison with measured results.

## The Frequency Doubler

Experimental measurements of the performance of a single-device FET frequency doubler were carried out using the arrangement shown in Fig. 1. The frequency doubler consists of a packaged, medium-power FET from RCA Labs., mounted in a microstrip fixture with the source grounded and with the dc-bias provided through bias-tees. The input (gate) and the output (drain) ports are connected to a 4 GHz signal source and a 50 ohm load respectively through lossless tuners. The purpose of the tuning networks is to optimize the output power at the desired frequency (in this case the second harmonic at 8 GHz); in addition, the output tuning network serves as a high-pass-filter, improving the spectral purity of the output. The remainder of the components in the set-up of Fig. 1 are for monitoring the input and output signals.

Several of the following performance parameters of the frequency multiplier may be of interest in any given application:

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(a) Multiplication Gain (MG), which is the ratio of the desired harmonic output power to the fundamental input power ($P_n/P_{in}$).
(b) Efficiency ($\eta$), which is the ratio of the harmonic power output to the dc power input ($P_n/P_{dc}$).
(c) Multiplication nonlinearity, which may be specified as the input power level at which the multiplication gain increases ("gain expansion") or decreases ("gain compression") by a given amount (usually 1 dB) with respect to MG at some nominal power level.
(d) Spectral purity ($P_n/P_m$), which is the ratio of the desired (n-th) harmonic to an undesired (m-th) harmonic power output.
(e) Bandwidth (B), over which the input signal frequency can be varied without degrading the multiplication gain beyond a specific amount.

In addition to the above parameters, which were measured, many other performance parameters may also be of interest, including the stability, noise characteristics, intermodulation characteristics, thermal characteristics, and sensitivity to operating conditions such as bias and temperature.

A representative set of measured performance parameters is shown in Fig. 2. Figures 2a and 2b show the dependence of the multiplication gain on the dc bias voltages at gate and drain terminals respectively. Fig. 2c shows the variation of multiplication gain with the power level of the input signal. DC-to-harmonic power efficiency is not separately plotted because it can be calculated from MG, $P_{in}$, and $P_{dc}$; $P_{dc}$ can be determined from dc drain voltage and current; and the drain current in turn is determined from the dc drain-to-source characteristics of the FET, given the dc bias voltages $V_{DS}$ and $V_{GS}$. The gain variation of Fig. 2c is typical in that the multiplication gain initially increases as the device is more strongly driven, reaches a broad maximum, and then decreases typically by 1 dB for a 3 dB increase in input signal. The spectral purity is strongly dependent upon the tuning network which acts as a filter; in all cases, the tuning could be adjusted to make $P_2/P_1$ exceed 20 dB, with the higher harmonics being still weaker. The bandwidth of the multiplier (under fixed tuning conditions) is also totally dependent upon the tuning network and does not describe an intrinsic property of the frequency multiplier. The FET device itself is inherently broadband, and frequency multiplication is limited only by the output cutoff frequency.

The best frequency doubler results, obtained from the single RCA device used, include a multiplication gain MG of -3 dB with a second harmonic power output of 25 mw and an efficiency of 15%.

For higher power frequency multiplication requirements, it is possible to design a multi-device circuit in which the device nonlinearity is exploited to further enhance the multiplication gain. An example of a two-device, push-pull type circuit is shown in Fig. 3. In this circuit, two frequency doublers, each identical to the one shown in Fig. 1, are connected in parallel through 3-dB couplers at the input and the output ports. A multiplication gain of +1 dB was measured with such a set-up when the biasing and tuning were adjusted for maximum gain, which is an improvement of 4 dB above the single-device circuit. The optimum dc bias was also different and was $V_{GS} = -7$ V and $V_{DS} = 7$ V. We emphasize that such an arrangement is not a simple power combining scheme with two independent multipliers; in linear power combining of 2 devices, the power output is increased by 3 dB (minus the combining loss of typically 0.25 dB due to couplers) but the multiplication gain is not.

## Nonlinear Model for FET

A field-effect transistor has a number of different independent sources of over-all device nonlinearity: the device nonlinearity arising from the nonlinear capacitive and resistive effects at the gate junction, the field-effect nonlinearity resulting in the nonlinear transconductance and pinchoff, and the nonlinear current transport in the channel due to velocity-saturation effects. These different nonlinearities have been utilized in different applications, and some are negligible for certain ranges of operating conditions; for example, three different FET mixers, each based on a different mechanism of nonlinearity, have been reported.[3-5] Each of the above three sources of nonlinearity is incorporated in the present model, shown in Fig. 4.

The nonlinearity due to the gate-source junction can be thought of as a nonlinear R-C transmission line. It has been modeled by a lumped $R_iC_{gs}$ network where the capacitance is a function of the instantaneous value of $v_{GS}$, the gate-to-source voltage, as for an abrupt junction varactor. The resistive nonlinearity due to the field effect has been modeled in two steps. First, the effect of the voltage $v_C$ across the capacitor $C_{gs}$ on the channel is doubly clipped:

$$v_1 = \begin{cases} V_P & \text{if} \quad v_c < V_P \\ v_c & \text{if} \quad V_P < v_c < V_F \\ V_F & \text{if} \quad v_c > V_F \end{cases}$$

where $V_F$ is a small positive voltage representing the forward gate bias above which the dc drain characteristics are uninfluenced, and $V_P$ is the (negative) pinchoff voltage. Second, the clipped voltage $v_1$ controls a current source, with a nonlinear transfer characteristic:

$$i_D = I_{DSS}\left(1 - \frac{v_1}{V_P}\right)^2 \tanh\left(\frac{\beta v_{DS}}{v_1 - V_P}\right)$$

where $I_{DSS}$ is the saturated dc drain current at zero gate bias and $\beta$ is a constant, typically about 1.2, chosen to match the drain characteristics. This also accounts for the channel saturation nonlinearity by incorporating the drain-to-source voltage ($v_{DS}$) dependence in the drain current $i_D$. The drain resistance $R_o$ and the drain-to-source capacitance $C_{ds}$ are treated as linear circuit elements. To this model may be added other passive, linear circuit elements representing the extrinsic and parasitic elements associated with the device.[6]

Note that the proposed FET model is quasi-static in nature and it has only two time-invariant, nonlinear elements $C_{gs}$ and $i_D$, which are instantaneous functions of the voltages $v_C$ and $v_{DS}$. (Similar assumptions have been proposed by others[7] in a different context.) Furthermore, in the interest of tractable analysis, the model ignores some elements (such as the feedback capacitor) and the nonlinearity of other elements (such as the drain resistance $R_o$). Finally, the model is proposed (and is later shown to be useful) only for very-large-signal (class B type) operating conditions, as would be typical in a frequency multiplier; obviously it will yield poor results when used for small-signal calculations. Although highly simplified, the model yields frequency-doubler characteristics which agree with observed results.

## Calculation of Frequency-Multiplier Performance

As expected, and readily verified experimentally, the performance of the frequency multiplier is strongly dependent on the linear circuits at the input and the output ports of the FET. These circuits must be modeled in order to calculate the performance parameters. The idealized circuit model of Fig. 5 is chosen both for ease of calculation and to obtain results that are not specific to an arbitrary choice of model parameter values. The ideal (very high Q) filters shown in the figure incorporate the parasitic elements of the device and are assumed to present a short-circuit between their terminals at all frequencies except one at which they present an open circuit.

The doubler performance calculated from this model for a representative set of FET parameters and operating conditions is shown in Fig. 6. The variation of the multiplication gain is similar to the measured behavior shown in Fig. 2. This leads to the possibility of using the proposed model for optimizing the doubler performance and determining the optimum operating conditions. This work is presently in progress.

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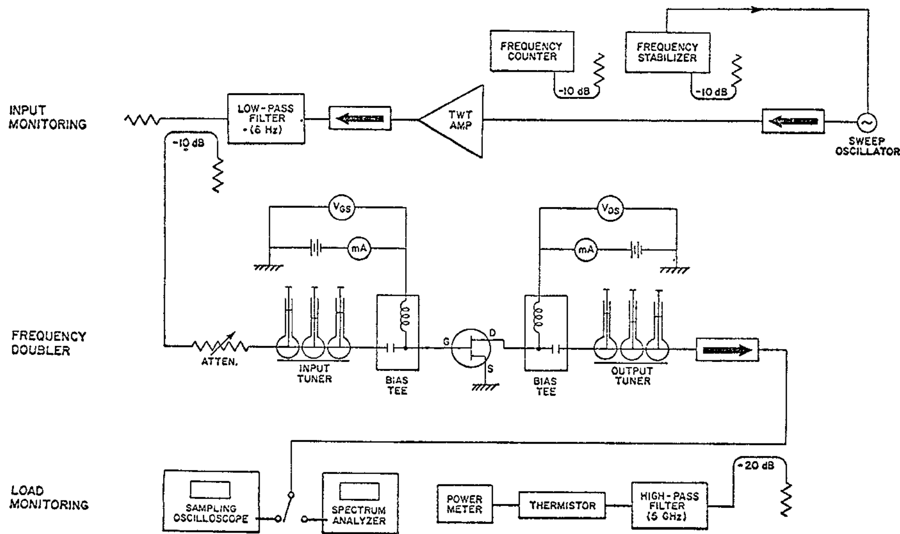


Fig. 1. Experimental arrangement for the measurement of the performance of a 4 GHz-to-8 GHz FET frequency doubler.

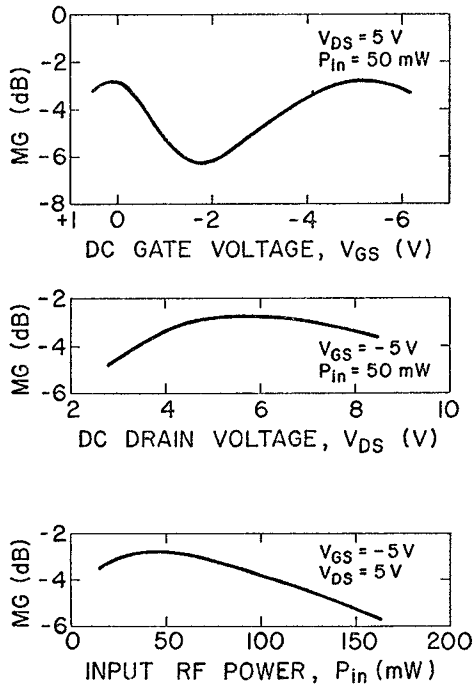


Fig. 2. Multiplication gain (MG) of the 4 GHz-to-8 GHz frequency-doubler using an RCA device, as a function of operating conditions.

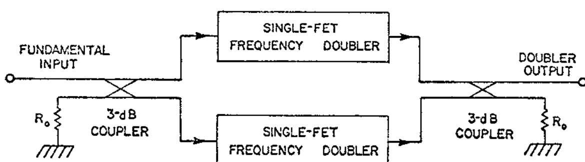


Fig. 3. Experimental arrangement for the dual-FET 4 GHz-to-8 GHz frequency-doubler.

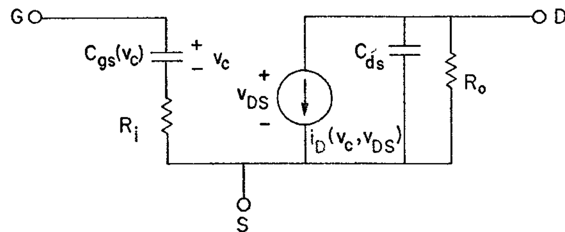


Fig. 4. Equivalent circuit model of a microwave GaAs FET, incorporating the nonlinearities due to the gate junction, field-effect, and channel saturation.

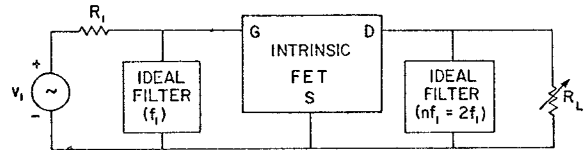


Fig. 5. Model of the frequency-doubler, with idealized input and output circuits.

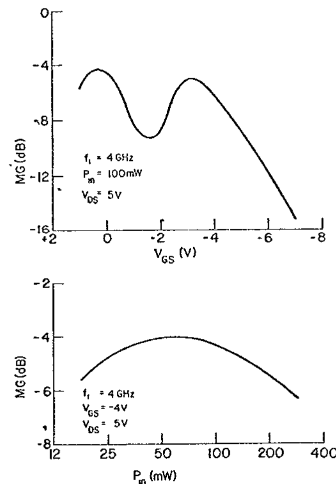


Fig. 6. Dependence of the frequency-doubler multiplication gain on the dc gate voltage, and the input power level as calculated from the nonlinear FET model.