Late Paper

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NOISE IN HIGH SPEED DIGITAL SYSTEMS

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Abstract -

This paper surveys the characterization and sources of noise in digital systems. The principal methods of characterizing noise in digital systems, including jitter and bit-error rate specifications, are explained, and the manner in which these are produced is described. The various sources of noise generated within, and coupled into, digital circuits are briefly reviewed. Design guidelines for minimizing the effects of noise are thus developed.

I. INTRODUCTION

With the rapid growth in the number of available digital microwave components, and their application to digital systems operating at clock speeds in excess of Gigabits/s, it has become necessary for microwave engineers to understand the digital circuits and their limitations. One such limitation is caused by "noise" in digital systems, a term which is usually loosely defined to include the degradation of digital signals due to the generation of noise within the circuit, as well as the interference coupled into the circuit through various means. While these physical sources of internally generated noise and the externally generated interference are the same as those in analog microwave circuits, the manner in which the noise in digital systems is quantitatively specified, and its influence on the system performance, are very different. This paper is a broad survey of the subject of noise in digital systems for microwave engineers.

Although the noise insensitivity of digital circuits was one of the major reasons for the replacement of analog circuits by digital circuits in communication, instrumentation, and control applications over the years, the digital circuits are not totally immune to noise. As digital systems operating at higher and higher speeds are designed, the problem of noise in digital systems becomes more apparent, partly because the higher speed devices respond more readily to noise transients, and partly because the coupling of externally generated noise into the circuit via circuit parasitics becomes more efficient at higher frequencies. Consequently, noise considerations must be included in the design of microwave digital systems, as has long been the case for analog systems. The purpose of this paper is to survey the characterization, origin, and minimization of noise in high-speed digital circuits and systems.

II. NOISE CHARACTERIZATION

Given the diversity of digital circuits, it is clear that several different methods of noise characterization must be used for digital circuits, depending on the nature and function of the circuits. This situation is similar to that in analog circuits where various measures for characterizing noise are used, such as noise figure for linear amplifiers and two-ports, AM and FM noise spectra for oscillators and harmonic generators, and minimum detectable signal for detectors and receivers.

For a systematic study, the various parameters that have been used for the quantitative specification of noise in digital circuits will be classified into the following three types, based on the the feature of the digital signal that is influenced by noise: the logic value, the amplitude, or the phase.

(1) Error Rate.

Conceptually the simplest effect of noise in a digital circuit is the logic error, which occurs when the presence of noise causes a change in the logic state of the digital circuit. A quantitative measure of the tendency of the circuit to cause such an error is the "probability of error", often denoted by P_E; this is the probability that the digital signal at the output of the circuit is logically incorrect. When the digital signal is a binary signal (having only two possible states), this probability is sometimes called the probability of bit error. When multiplied by the rate at which the circuit generates or processes the bits, it gives the error rate, defined as the number of errors per unit time. The error rate is the primary measure of the noise performance of digital communication systems.

(2) Amplitude (or Level) Fluctuation.

Another effect of noise in digital circuits

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is the fluctuation in the analog value of the digital signal, even while the logic state does not change. Level fluctuations are defined as the random variations in the output voltage of the digital circuit with time while it is maintained in a single logic state, or as the circuit is brought back to that state from time to time. This variation is important only in those circuits where the analog value of the level is used for some purpose, for example in circuits involving digital-to-analog conversion, or in relaxation oscillators where the voltage amplitude governs the rate at which a capacitor is charged. Furthermore, the presence of large level fluctuations increases the probability of error, since it decreases the tolerable level of noise that can be present before an error occurs.

(3) Time Jitter.

In many digital circuits, the noise manifests its effect in the timing (i.e., the phase) rather than in the amplitude of the signal. Jitter is defined as the short-term variation of the significant instants of a digital signal from their ideal position in time. The significant instant can be any well-defined point on a digital signal waveform, such as the instant at which a specified threshold value is reached. As a result, the jitter is a continuous random variable (the amount of deviation in the occurrance of the significant instant), defined on a discrete domain (i.e., once in each cycle). Alternatively, its successive values can be viewed as samples of a continuously time-varying random signal which phase modulates the otherwise ideal timing signal. Being a random variable, the magnitude of jitter can be specified in a number of ways, such as the r.m.s. value.

III. SOURCES OF NOISE

The noise performance of a digital circuit is determined by a variety of noise sources. For a systematic study, these will be classified into two groups. The first group consists of noise which is spontaneously generated within the circuit, while the second group includes noise signals generated outside the circuit, and then coupled into the circuit.

The spontaneously generated noise in the circuit arises from a number of sources. The first is thermal noise, which is present in all resistive circuit elements or regions of a device, such as the channel region of a field-effect transistor. The mean square value of the thermal noise voltage is given by Nyquist's theorem :

$$\overline{v_n^2} = 4\,k\,T\,R\,B$$

where k is Boltzmann's constant, T the temperature of the resistive element, R is the resistance of the linear resistor, and B is the bandwidth over which the thermal noise is operative, given the bandwidth of the circuit. When applied to FETs, the appropriate channel temperature must be used, and corrections for the nonlinearity of the channel must be included.[1]

The second source is shot noise, contributed by junction diodes and transistors. Each independent component I of the total current crossing a junction barrier contributes a mean square current

$$\overline{i_n^2} = 2\,q\,I\,B$$

over abandwidth B, where q is the magnitude of the charge of an electron. A third source is the 1/f noise, having a noise spectrum of the form 1/f. The mean square value of the noise voltage or current due to this source will be proportional to the square of the bias current flowing in the device under consideration, as well as to the number of carriers involved in the region in which this noise is generated. The primary source of this noise in digital circuits is the MOSFET. Burst or "popcorn" noise present in bipolar noise is also a low-frequency phenomenon; it occurs for short durations at intervals, thus having a random pulse like characteristic. Finally, there is also noise caused by high-energy radiation, such as alpha particles and cosmic radiation, which can create charge carriers by ionization. The errors created by this noise are called "soft noise", since they are non-recurring and there is no damage to the circuit.

The externally generated interference can couple into the digital circuit in three principal ways. First, the parallel interconnect lines, which are inevitably present, serve as coupled transmission lines, and thus introduce unwanted signals in the circuit, called "cross-talk". Second, the parasitic impedances present in the ground and power supply lines also introduce coupling between circuits. Finally, at very high speeds, a radiative coupling between digital circuits is also possible, wherein one circuit acts as a transmitting antenna and another as a receiving antenna. Although the cross-talk introduced by the above three mechanisms is not truly a random signal, it can be treated as such for circuits with large number of inter-coupled elements, since the cross-talk is then a superposition of a large number of coupled signals. The effect of cross-talk can be modelled as a random signal, by assigning an equivalent noise source as the source of cross-talk, and characterizing it in terms of parameters like r.m.s. value[2]

IV. NOISE IMMUNITY

In order to relate the noise voltages present in a circuit to the logic error rate described earlier, it is necessary to consider another attribute of digital circuits, namely the noise immunity. Unlike linear circuits, a digital circuit has the ability to prevent noise at its input from being transferred to its output. The noise immunity is a measure of that ability, and is quantitatively measured in terms of the magnitude of the signal (e.g., a voltage) that can be applied to an input of the circuit without causing the output of the circuit to change its logic state. The noise immunity of an entire system originates from, and is a complex function of, the noise immunity of individual digital circuits within it.

For a single logic gate, the noise immunity is directly related to the noise margin of the gate, defined as the minimum difference between the voltage available at the output of that circuit in a given logic state, and the voltage required at the input of the circuit (assumed to be an identical gate) driven by the given gate in order to have the logic state correctly interpreted. There are a number of ways this noise margin is defined and calculated for given circuit; for example the knowledge of the static transfer characteristic of an inverter gate is sufficient to calculate the static noise margin of the gate by a simple geometrical construction. The relationships between the several definitions of noise margin have been discussed in the literature.[3]

It is clear from the definition that the noise margin is small when the logic voltage swing is small, or when there is a large scatter in the values of device parameters (like pinch-off voltage of the FETs) or of temperature within a digital system. In addition, the noise margin of a logic gate is a function of the loading and fan-out of the gate. In addition, the variations of the signal amplitude within the circuit (e.g., due to voltage drops along bus-lines) will further reduce the noise immunity of the overall circuit.

V. PROBABILITY OF LOGIC ERROR

The basic idea behind the calculation of the probability of logic error in a digital circuit can be conveyed by considering a highly simplified case of a digital system shown in Fig. 1 below.

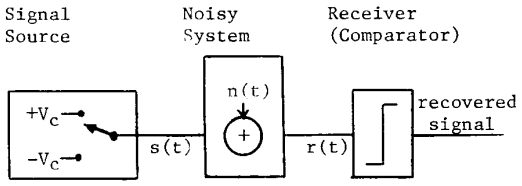

Fig. 1. An idealized digital system for defining the probability of error.

This system can be viewed as a model of a digital communication system in which the following simplifying assumptions have been made :
(i) The digital signal is a binary signal, limited to two choices S_1 and S_2.
(ii) The signals S_1 and S_2 are dc voltages (base-band operation).
(iii) The digital signal s(t) is contaminated by additive white Gaussian noise (AWGN), resulting in a noisy signal r(t) = s(t) + n(t), where n(t) is the noise having the Gaussian amplitude probability function

$$p_n(x) = \frac{1}{\sqrt{2\pi}\ a} \exp\left(\frac{-x^2}{2a^2}\right)$$

where a is the r.m.s. value of the noise n(t) over the effective noise bandwidth of the circuit.

(iv) The noisy signal r(t) is used to deduce whether s(t) was S_1 or S_2 with the help of a receiver, which in this case is simply a comparator having a zero threshold voltage; i.e., the decision rule is

$$s(t) = \begin{cases} S_1 & \text{if } r(t) > 0 \\ S_2 & \text{if } r(t) < 0 \end{cases}$$

For such a simple system, the error in the recovered signal can occur in two mutually exclusive ways :

(i) The signal was S_1, but was judged to be S_2 (i.e., $s(t) = +V_c$, but $r(t) < 0$).
(ii) The signal was S_2, but was judged to be S_1 (i.e., $s(t) = -V_c$, but $r(t) > 0$).

The total probability of error is therefore the sum of the probabilities of the above two events :

$$P_E = \text{Prob}\ (\ n(t) < -V_c;\ \text{while } s(t) = +V_c\ ) + \text{Prob}\ (\ n(t) > +V_c;\ \text{while } s(t) = -V_c\ )$$

If the signal source s(t) takes the values S_1 and S_2 with equal probabilities, the probability of error can be found by integrating the probability density function for n(t) :

$$P_E = \int_{V_c}^{\infty} \frac{1}{\sqrt{2\pi}\ a} \exp\left(\frac{-x^2}{2a}\right) dx = \frac{1}{2} \operatorname{erfc}\left(\frac{V_c}{\sqrt{2}\ a}\right)$$

where erfc (.) is the complimentary error function.

The above calculation of P_E can be generalized in many directions. For example, the signal s(t) may be an encoded, encrypted, modulated, multiplexed, or otherwise modified signal, rather than just dc levels $+V_c$ and $-V_c$. In this case, the comparator must be replaced by a more involved receiver, based on selecting an output depending on whether the noisy signal r(t) is "closer" to one or the other expected signals $S_1(t)$ or $S_2(t)$. Second, the signal s(t) may be an M-ary signal, rather than a bianry signal. Third, the detector may be noncoherent, so that it is necessary to select an energy detector as the receiver. Other such generalizations can be found in the literature.[4] In all cases, the probability of error P_E is a function of the signal-to-noise ratio, which was $(V_c/a)^2$ in the above simplified system.

VI. TIME JITTER

A digital circuit can introduce jitter in its output signal (or add to the jitter already present in its input signal) through a variety of mechanisms. Some of the common mechanisms are as follows.

(1) Jitter Due To Timing Circuit. In some digital circuits, such as relaxation oscillators, the switching time of a digital circuit depends on the instant at which some analog voltage reaches a threshold value (such as the voltage across the capacitor in an R-C timing circuit of a multivibra-

tor). It is clear that the fluctuations in the charging of the capacitor, due to the noise in the active device supplying the charging current, or the thermal noise of the resistor R, will produce a corresponding fluctuation in the instant of transition at the output of the circuit. Detailed numerical calculations of this jitter are available in the literature, and suggest the quantities that can be controlled to reduce the jitter.[5]

(2) Jitter Due To Finite Rise Time Of Input Signal. If the input signal of a digital circuit has a finite rise time, the presence of additive noise would displace the time instant at which the total signal reaches the threshold value causing transition at the output. This is illustrated in Fig. 2 below, where the effect is exaggerated for clarity.

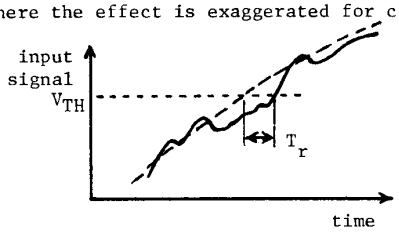

Fig. 2. Jitter caused by noise superimposed on a signal with finite rise time.

Quantitative estimates of this jitter can be made as follows. If

n(t) = the additive noise superimposed on signal,
V_{TH} = the threshold value of the input signal at which a transition occurs at the output,
m = the rate of rise (slope) of the signal near its threshold value,

then the jitter in the instant of output transition can be determined from

$$T_r = \text{zero-crossing time of } m.t + n(t) - V_{TH}$$

The statistics of jitter can therefore be found from a knowledge of the input signal (i.e., m), the circuit (i.e., V_{TH}), and the noise (i.e., n(t)).

(3) Jitter Due To Finite Propagation Delay. The propagation delay of a logic gate is a sum of several components, each of which can be traced back to, or represented as, a capacitive element which requires charging.[6] The capacitive elements include load capacitance, internal capacitance of active devices, and parasitic capacitances in the circuit or interconnect lines. The charging time of these capacitive elements will fluctuate due to the fact that the initial state of the capacitors fluctuates due to the noise voltages present in the circuit. Perhaps the most direct proof of this statement is the jitter in the output of a ring oscillator (a chain of odd number of inverter gates connected in a closed loop), in which the oscillator frequency is governed by the total propagation delay of the gates in the loop.

(4) Jitter Due To Signal Regeneration. Many types of digital regenerators, or other types of timing recovery circuits, are used in communication systems. The nonlinearity of the circuits used in such systems causes jitter through amplitude-to-phase conversion, intersymbol interference, and other such phenomenon. This jitter is signal-dependent (called "pattern dependent"), and it accumulates in systems with many regenerators or multiplexers.[7-8]

Jitter can have a variety of effects on the performance of the digital system. As an example, jitter in sampling can cause unwanted spectral components in an analog signal that has been digital filtered.[9] Jitter in synchronizer circuits can cause bit errors.[10]

VII. LOW-NOISE DESIGN

Several of the design guidelines for low-noise design can be deduced from the above discussion. These include the proper selection of DC bias point for active devices, placement of interconnect lines and circuit segments with respect to each other, reduction of parasitics, and provision of low ac impedance path between power supply terminals and the circuit, as well as to the ground terminals. Alternative design methods yielding higher noise margin in logic gates can be used where high noise immunity is necessary.

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