TABLE I
RESULTS OF MEASUREMENTS ON SEVERAL MULTIPLIER CIRCUITS; THE POWER-DELAY PRODUCT EQUALS THE POWER DISSIPATED BY ONE CELL TIMES THE TIME NEEDED TO PRODUCE ONE OUTPUT BIT (THIS IS ONE CLOCK PERIOD)

Run number		XEP 10	XER 6	XEP 9	XER 14
Supply voltage	(V)	5	5	7	10
Current drawn	(mA)	11	23	35	100
Power dissipation	(mW)	55	115	245	1000
Max. clock frequency	(MHz)	2.5	5	7	7
Power delay product per bit	(nJ)	1.83	1.92	2.92	11.9
V_T-load	(V)	-1.1	-1.9	-2.2	-3.8
V_T-driver	(V)	+1.2	+0.5	+0.4	+0.5
Substrate bias	(V)	/	-2.	-2.	-2.

given by current source T_2, is increased. This is what happens when the threshold voltage of T_2 is increased. A further increase of the clock frequency needs a layout change. The aspect ratio of the pass transistors must be made larger than unity. This can be done with minor changes in total layout. The output stage was designed to directly drive one TTL-gate (for XER 6 and XER 10). This stage is not influencing the operating speed when the load capacitance is less than 70 pF.

From Table I one can conclude that the load device threshold voltage has to be kept close to -2.2 V in order to get a high speed operation for a low power dissipation (for the present layout rules). It is possible to change the channel length of all transistors by decreasing the metal line width. For a 5-μm wide metal and using the process steps of XER 9, a maximum bit rate of 14 MHz is possible for a power dissipation of about 500 mW.

The NENDEP multiplier performance can be compared with other realizations. Kane [7] described a bipolar multiplier operating at 20 MHz using 10-μm design rules. In his approach extra off-chip shift registers have to be added. The power dissipation equals 37.5 mW per bit for this bipolar circuit, while the NENDEP multiplier (run XER 9) only dissipates 10.5 mW per bit. The power-delay product per bit of the bipolar circuit equals 1.9 nJ, while for the NENDEP version this value equals 2.9 nJ, but no external circuitry is needed here.

From this one can conclude that the bipolar version is faster but has a larger power dissipation. Therefore the NENDEP technology seems to be better suited for the extension of the multiplier to more bits in series or to a fully integrated second order digital filter.

A CMOS/SOS multiplier has been reported by Hampel *et al.* [8]. This circuit operates at 18-MHz clock rates; the output bit rate is 9 MHz. Since layout rules and details on technology are not available it is difficult to evaluate these performance values.

VI. CONCLUSIONS

A 12-bit pipeline multiplier is integrated in the NENDEP technology. The circuit can be made fully TTL-compatible. When a back-gate bias is applied a bit rate of 5 MHz is allowed for a supply voltage of +5 V. The capacitive clock loading is only 20 pF per phase. This small value results from the layout in which only the pass transistor gates are connected to the clock lines.

When the threshold voltage of the load devices is increased (in absolute value) the maximum clock frequency is 7 MHz. This value is obtained for a layout using 10-μm line widths and thus 10-μm channel lengths. At 7 MHz the minimum power dissipation equals 245 mW. A capacitor of maximum 70 pF can be driven. Decreasing the channel length to 5 μm (while keeping all other parameters the same) would lead to a 14-MHz operation for a power dissipation less than 500 mW. This dissipation level allows for an extension of the circuit to a second-order digital filter stage without causing too much of a cooling problem.

ACKNOWLEDGMENT

The author would like to thank the I.W.O.N.L. for his fellowship.

REFERENCES

[1] S. L. Freeny, R. B. Kieburtz, K. V. Mina, and S. K. Tewksbury, *IEEE Trans. Circuit Theory*, vol. CT-18, no. 6, pp. 702–711, 1971.
[2] L. B. Jackson, J. F. Kaiser, and H. S. McDonald, *IEEE Trans. Audio Electroacoust.*, vol. AU-16, pp. 413–421, 1968.
[3] J. R. Verjans and R. J. Van Overstraeten, "NENDEP—A simple N-channel MOS technology for logic circuits," *IEEE J. Solid-State Circuits*, vol. SC-10, pp. 212–218, Aug. 1975.
[4] A. Landauro, Ph.D. dissertation, Mons, Belgium, 1973.
[5] M. Van Cappellen, internal report.
[6] J. R. Verjans and R. J. Van Overstraeten, "Electrical characteristics of boron-implanted n-channel MOS transistors for use in logic circuits," *IEEE Trans. Electron Devices*, vol. ED-22, pp. 862–868, Oct. 1975.
[7] J. Kane, in *Int. Solid-State Circuits Conf., Dig. Tech. Papers*, 1976, pp. 16–17.
[8] D. Hampel, K. E. McGuire, and K. J. Prost, "CMOS/SOS serial-parallel multiplier," *IEEE J. Solid-State Circuits*, vol. SC-10, pp. 307–314, Oct. 1975.

Microwave Characterization of GaAs MESFET and the Verification of Device Model

JOHN F. COOPER AND MADHU S. GUPTA

Abstract—**The elements in the small-signal equivalent circuit model of a microwave GaAs MESFET have been related to the device parameters (i.e., device structure, semiconductor properties, and operating point) by device theories. This equivalent circuit is experimentally verified by small-signal 3-GHz microwave measurements at room and liquid-nitrogen temperatures. The method used for determining the values of equivalent circuit parameters is briefly described.**

I. INTRODUCTION

Several theoretical models of the GaAs MESFET [1] operating at microwave frequencies have been proposed and are reviewed in [2]. One of the most extensive one-dimensional small-signal models is that of Pucel *et al.* [2]. The purpose of the present study is to experimentally carry out a complete characterization of a microwave GaAs MESFET and thereby

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to determine the applicability and accuracy of this model. The device model in [2] yields only the intrinsic elements and the device parasitics related to the active region. Therefore, a comparison of the model with measurements required that a detailed modeling and experimental measurement of the FET parasitics, package, and circuit fixture be carried out in order to determine the active region parameters by de-imbedding. A second purpose of the present work is to describe the method of measurement or calculation of device parasitics, and the model used for de-imbedding.

The GaAs MESFET characteristics at low temperatures are of interest because the devices are known to improve in noise performance upon cooling. The small-signal microwave measurements and verification of the small-signal model were therefore carried out at room temperature as well as at liquid-nitrogen temperature. A comparison of the measured and calculated S-parameters shows an approximate agreement and lends support to the theoretical model. These results, as well as the technique used to determine the two sets of S-parameters, are summarized here. Complete details of the work are available as a thesis [3].

II. Device and Circuit Models

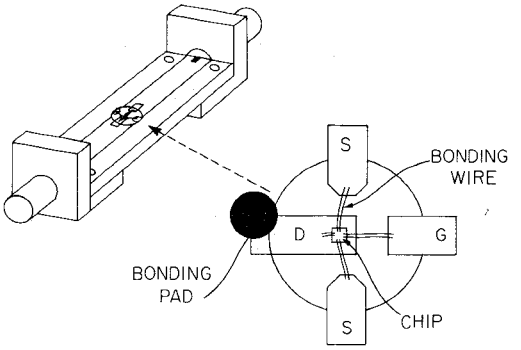
The device used in the present study is the 1-μm gate length GaAs FET made by the Hewlett-Packard Company, Palo Alto, CA. The device is packaged and then mounted in a microstrip test fixture shown in Fig. 1(a). This entire circuit is modeled as shown in Fig. 1(b). The intrinsic FET, together with its chip parasitics due to the substrate and metallizations, will be referred to hereafter as the extrinsic FET. The outer four-port, representing the FET package (i.e., the bonding wires and the bonding pads), is assumed lossless. Detailed circuit models were developed for each of the networks shown in Fig. 1(b). Lumped circuit models are used for the intrinsic elements, parasitic elements, and package due to their small dimensions, while a distributed circuit model is used for the two separate two-ports representing the microstrip transmission lines and connectors of the test fixture. These models are shown in Fig. 2 and are briefly discussed here.

1) *Intrinsic Elements:* The intrinsic FET model of Fig. 2(a) is identical with that used by many authors, and employed in [2]. The transconductance of the device g_m, the output resistance R_d, the gate-to-source capacitance C_{gs}, and the gate-to-drain capacitance C_{gd} have been calculated analytically from the FET model in [2]. The undepleted channel resistance R_i is the only element in the intrinsic model which is not directly calculated.

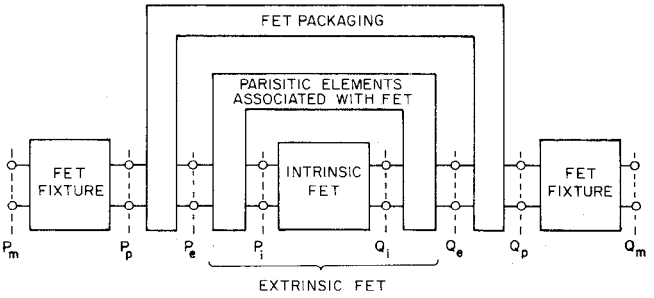
2) *Extrinsic Elements:* The parasitic elements associated with the FET chip are shown in Fig. 2(b). The three resistances R_m, R_{dr}, and R_f, in series with the gate, drain, and source terminals, respectively, are due in part to the contact resistance at the metallization and in part to the bulk resistance of the semiconductor. The capacitors C_{gd1}, C_{gs1}, and C_{ds1} arise due to the capacitances between the various metallizations on the chip.

3) *Package Parasitic Elements:* The packaging of the FET adds three sets of parasitics which are shown in Fig. 2(c). They include the inductors L_1, L_2, L_3 representing package leads and bonding pad inductances, the capacitors C_1, C_2, C_3 representing capacitances between the three bonding pads, and inductors L_4, L_5, L_6 representing bonding wire inductances.

4) *Test Fixture Parasitics:* The fixture model of Fig. 2(d) on one side of the packaged device consists of two transmission lines of lengths l_3 and l_1 representing the connector and the microstrip, respectively, and an inductor L_{f5} representing the interconnection of the two lines. The lines are taken as lossless and the line loss is separately accounted for by the attenuator A_{s1}. A similar model is used on the other side of the packaged device.

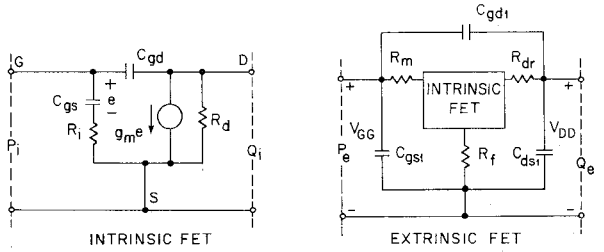


(a)

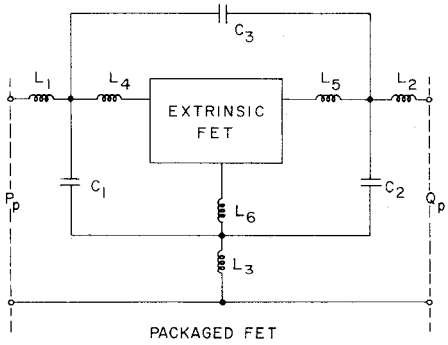


(b)

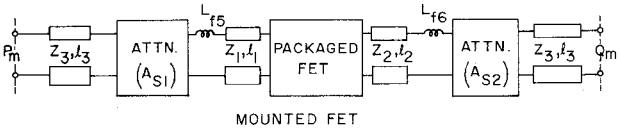
Fig. 1. (a) Packaged FET device mounted in a test fixture. (b) Port-wise models for the intrinsic FET, device parasitics, package, and fixture circuit.



(a) (b)



(c)



(d)

Fig. 2. Detailed circuit models for (a) the intrinsic FET, (b) the extrinsic FET, which includes the device parasitics, (c) the packed FET, and (d) the packed FET mounted in the test fixture.

III. Calculated S-Parameters

The S-parameters of the extrinsic FET (between reference planes P_e and Q_e) are easily calculated from the circuit models of Fig. 2(a) and 2(b), in terms of the eleven circuit elements used in these models. The values of these eleven lumped circuit elements are therefore to be calculated. Only four of these elements are essentially related to the mechanism of the device and are predicted by theoretical models of device operation. The rest had to be separately estimated or obtained by measurements. The determination of these elements is briefly discussed here.

1) *Theoretically Calculated Parameters:* Four of the five intrinsic elements, g_m, R_d, C_{gs}, and C_{gd}, can be calculated from the closed form analytical expressions derived from the FET model [2]. These expressions will not be reproduced here. However, they relate the four elements to the semiconductor material properties (namely, low-field mobility, saturated carrier velocity, doping density or resistivity of the epitaxial layer, dielectric constant, and built-in potential), device structural dimensions (device width, gate length, source-to-gate and gate-to-drain interelectrode spacings, and epitaxial layer thickness), and device dc bias (V_{DD} and V_{GG}). Of these, the material properties are temperature sensitive, so that the four element values have to be calculated separately for room temperature and for liquid-nitrogen temperature. The calculated values of these elements are shown in Table I for the specified biasing conditions and temperatures.

2) *Separately Determined Parameters:* Of the six device parasitic elements, the three electrostatic capacitances were estimated from a knowledge of the geometry of metallizations on the chip, with corrections applied for fringing. In the FET device employed here, the drain terminal was connected to the metallization under the substrate, so that the capacitances C_{gd1} and C_{ds1} are significant (estimated to be 0.015 pF and 0.06 pF, respectively) while C_{gs1} is negligible. The three extrinsic resistances are measured by dc current and voltage measurements, treating the intrinsic FET as two p-n junctions across a conductive channel. R_f and R_m are measured by passing a forward current I_{gs} into the gate-source junction and measuring the resulting voltage at the floating drain with respect to source and gate, respectively, (neglecting the incremental resistance of a forward-biased junction):

$$R_f = \frac{\Delta V_{ds}}{\Delta I_{gs}}; \; R_m = \frac{\Delta V_{gd}}{\Delta I_{gs}}.$$

R_{dr} is similarly measured by forward biasing the gate-drain junction and measuring the voltage at floating source:

$$R_{dr} = \frac{\Delta V_{sd}}{\Delta I_{gd}}.$$

These measurements were made both at room temperature and at liquid-nitrogen temperature, and the values obtained are included in Table I. The last intrinsic element R_i is assumed to be negligible here; the effect of the bulk resistance of undepleted epitaxial layer under the gate electrode is accounted for in the measurement of R_m discussed earlier.

The scattering parameters of the extrinsic FET are calculated from the circuit models of Fig. 2(a) and 2(b) using the tabulated values of these eleven circuit elements at a desired frequency.

IV. Measured S-Parameters

All microwave measurements of S-parameters are made with a network analyzer at the ports of the microstrip fixture of Fig. 1(a), i.e., at reference planes P_m and Q_m. The fixture and the package were separately characterized from 2 to 4 GHz and the S-parameters for the extrinsic FET were determined by de-imbedding techniques. The determination of measured S-parameters thus consisted of the following four steps.

TABLE I
Calculated Values of the Equivalent Circuit Elements of the Extrinsic FET at V_{DD} = 4 V and V_{GG} = 0 and at 3 GHz

Element	Unit	Value	
		T = 300 K	T = 77 K
g_m	mho	0.053	0.0735
R_d	Ohm	1100	650
C_{gs}	pF	0.35	0.4
C_{gd}	pF	0.052	0.051
R_m	Ohm	9.3	5.1
R_f	Ohm	3.3	2.4
R_{dr}	Ohm	4.2	3.2
C_{gd1}	pF	0.015	
C_{ds1}	pF	0.06	
C_{gs1}	pF	0.0 (assumed)	
R_i	Ohm	0.0 (assumed)	

1) *Fixture Characterization:* The microstrip-to-coaxial adapter was characterized by effectively placing a short-circuit at its microstrip end, and measuring the input reflection coefficient as a function of frequency; the parameters l_3 and Z_3 of the model of Fig. 2(d) were then calculated to fit the measurements. The rest of the fixture was characterized by placing a short where the device package would be, and making similar measurements of reflection coefficients; the parameters Z_1, l_1, L_{f5}, and A_{s1} where estimated in this manner.

2) *Package Characterization:* The packaged device is replaced successively by three specially prepared calibration packages in which the FET chip is substituted by open, short, or through circuits between the gate, drain, and source terminals. The S-parameters of each of the resulting two-ports are measured as a function of frequency, and the package equivalent circuit elements of Fig. 2(c) are calculated to fit the measurements.

3) *Device Measurements:* With the packaged device placed in the fixture, the S-parameters are measured at ports P_m, Q_m at the desired frequency, temperature, and dc bias. The entire fixture was lowered in a Dewar of liquid nitrogen for low-temperature measurements.

4) *Parameter De-imbedding:* The S-parameters for the extrinsic device at ports P_e and Q_e were determined from the measured S-parameters at ports P_m and Q_m with the help of MARTHA, a network analysis computer program [4], using the previously established equivalent circuits of Fig. 2(d) and 2(c) for the fixture and the package. Details of measurements and calculations are available elsewhere [3].

V. Conclusions

1) *Model Validity*: The calculated and the measured S-parameters for the extrinsic FET are plotted together in Fig. 3 for comparison at 1) a fixed signal frequency of 3 GHz, 2) a fixed dc biasing point of V_{DD} = 4 V, V_{GG} = 0 V, and 3) two values of temperature, T = 300 K and 77 K. The validity and utility of the theoretical device model of [2] is evidenced by the approximate agreement, both at room temperature and at liquid-nitrogen temperature, between the measured (de-imbedded) and the calculated S-parameters. To put these results into proper perspective, it is essential to reemphasize the origin of calculated parameters. It might appear that a far

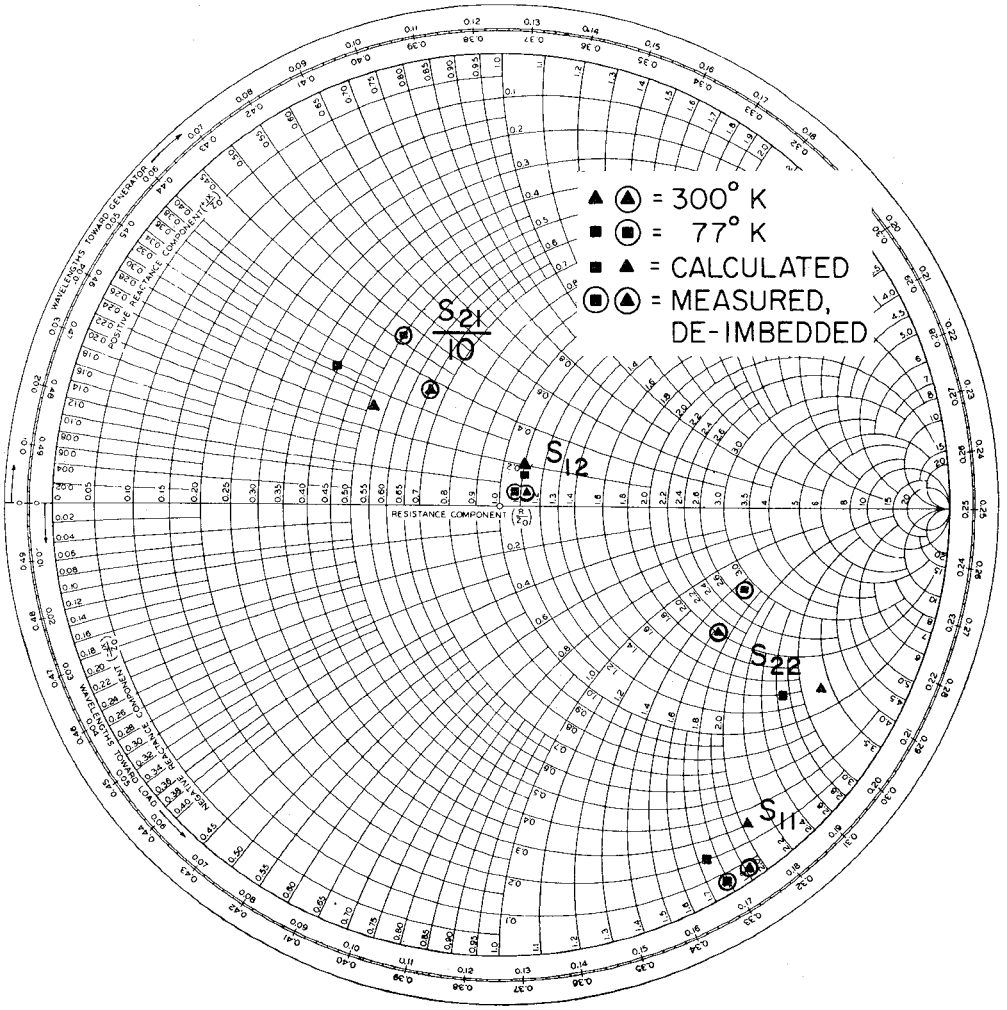


Fig. 3. Scattering parameters at the extrinsic FET ports at room temperature (triangles) and liquid-nitrogen temperature (squares) as determined by device model (uncircled) and by de-imbedding the microwave measurements made at fixture ports (circled).

better agreement between measured and calculated S-parameters has previously [5] been reported for Schottky-barrier FET's (see, for example, [5, figs. 2 and 3]). Note, however, that the calculated S-parameters in [5] were determined from an equivalent circuit, the element values of which were themselves selected to provide the best match between the calculated and measured S-parameters. The "agreement" therefore verifies only the usefulness of the form of equivalent circuit. In the present work, the element values in the equivalent circuit, and therefore the calculated S-parameters, are determined independently of the measured S-parameters. The approximate agreement therefore lends support to the physical model of the device used in the calculation of intrinsic parameters.

2) *Model Refinements*: The quantitative evaluation of the model of [2] shows some possibilities of refinement. Of the four scattering parameters for extrinsic FET, the discrepancy between calculated and measured values is largest for S_{22}. This difference arises, in part, from the value of R_d calculated from the theoretical model, which is high compared to the value based on dc characteristics. Another source of discrepancy may be the high value of C_{gd} calculated from the model; a lower value can be justified on the basis of more detailed physical models [6]. Finally, the theoretical model [2] employed here does not include the drain-to-channel internal-feedback capacitor (C_{dc} in [5]) which has been reported to be necessary for a good fit [7]. However, the model may be adequate for some purposes, and is useful due to its closed-form results.

3) *Package Parasitics*: A careful consideration of FET parasitics was essential for the above model verification, but is not novel and is not detailed here due to space limitations. A significant conclusion is that the device parasitics can be well-estimated by the present method. The method should therefore be useful in carrying out the adjustment of parasitics for optimization and in-package matching.

Acknowledgment

Thanks are due to the Hewlett-Packard Company for providing the devices and their details, and to Dr. R. Pucel of Raytheon for discussions regarding the FET model.

References

[1] C. A. Liechti, "Microwave field-effect transistors–1976," *IEEE Trans. Microwave Theory and Techniques*, vol. MTT-24, pp. 279–300, June 1976.

[2] R. A. Pucel, H. A. Haus, and H. Statz, "Signal and noise properties of gallium arsenide microwave field-effect transistors," in *Advances in Electronics*, L. Marton, Ed., vol. 38. New York: Academic, 1975.

[3] J. F. Cooper, *Characterization of a Microwave GaAs FET at Low*

Temperature, S. B. and S. M. theses, Dept. Elec. Eng. and Comput. Sci., Mass. Inst. Tech., Cambridge, MA, 1976.
[4] P. Penfield, Jr., *MARTHA User's Manual*, M. I. T. Press, Cambridge, MA, 1971.
[5] C. A. Liechti and R. B. Larrick, "Performance of GaAs MESFET's at low temperatures," *IEEE Trans. Microwave Theory and Techniques*, vol. MTT-24, pp. 376–381, June 1976.
[6] K. Lehovec and R. S. Miller, "Field distribution in junction field-effect transistors at large drain voltages," *IEEE Trans. Electron Devices*, vol. ED-22, pp. 273–281, May 1975.
[7] R. H. Dawson, "Equivalent circuit of the Schottky-barrier field-effect transistor at microwave frequencies," *IEEE Trans. Microwave Theory and Techniques*, vol. MTT-23, pp. 499–501, June 1975.

Comments on "A Low-Pass Biquad Derived Filter Realization"

CHARLES CROSKEY

In the above paper,[1] the author presents a biquad low-pass filter which requires only two operational amplifiers. The use of current differencing amplifiers for reduced operational amplifier count implementation of the biquad filter has been around for some time [1]. However, Mr. Brodie does not mention that the low-pass form is not the only filter that can be achieved. If one allows one additional resistor for biasing, a true bandpass output is available.

This is illustrated in the slightly altered configuration shown in Fig. 1. Conductance G_6 is used only for biasing, and for optimum biasing, should be chosen to be one half of G_3.

If we proceed with the analysis in the usual way, one finds

$$\frac{V_{bp}}{V_{in}} = \frac{-sG_2/C_1}{s^2 + sG_1/C_1 + G_4G_3/C_1C_2} \tag{1}$$

permitting one to identify

$$\omega_n = \sqrt{\frac{G_4G_3}{C_1C_2}} \tag{2}$$

and

$$Q = \sqrt{\frac{C_1G_4C_3}{C_2G_1^2}}. \tag{3}$$

The magnitude of the gain at resonance is $G_2/G_1 = K_{bp}$. Another constraint for optimum biasing is $G_4 = G_1 + G_2 = (1 + K_{bp})G_1$.

If a reduced spread in element values is desired, let

$$C_2 = C, \qquad C_1 = \frac{Q}{\sqrt{1 + K_{bp}}}C \tag{4}$$

and

$$G_1 = G, \qquad G_3 = \frac{Q}{\sqrt{1 + K_{bp}}}G. \tag{5}$$

A true low-pass output is also available from the other amplifier's output, but its dc gain is more limited, being $G_2/G_4 = G_2/(G_1 + G_2) = K_{lp}$, always less than one. One should also consider the gain of the amplifier whose output is not used. From Mr. Brodie's equation (6) we find that for a steady-state sine wave at resonance

$$T_x = K_{lp}Q^2(1 - j/Q) \tag{6}$$

so one must stay with low Q circuits to avoid saturation in this stage. For the circuit described here, the "other" amplifier output is the bandpass output which provides a gain at resonance of

$$K_{bp} = \frac{K_{lp}}{1 - K_{lp}} \tag{7}$$

which will be much easier to keep manageable when a highly peaked response is desired. Conversely, if the bandpass output is utilized, the low-pass output has a gain at resonance of

$$\frac{K_{bp}}{1 + K_{bp}}Q = K_{lp}Q \tag{8}$$

so care must still be exercised for large Q's.

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[1] J. H. Brodie, *IEEE J. Solid-State Circuits* (Corresp.), vol. SC-11, pp. 552–555, Aug. 1976.

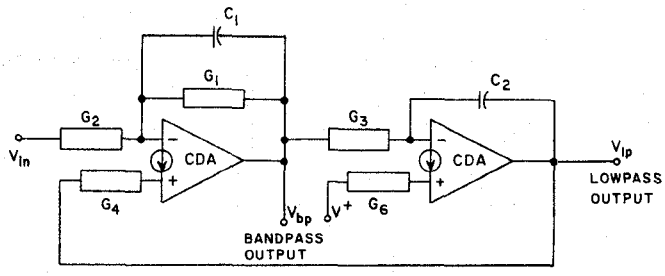

Fig. 1.

REFERENCES

[1] C. Croskey, "State-variable filter uses only two op amps," *Electronics*, pp. 98–99, March 21, 1974.

Author's Reply[2]

J. H. BRODIE

Dr. Croskey's state variable filter [1] is a modification of Thomas's biquad [2] which yields both bandpass and low-pass behavior. The circuit is well known to this author, and I have made an analysis of another modification of it (using the LM 3900) which appeared in print recently [3]. I did not reference this article at the time of writing the correspondence under discussion[1] since it ([3]) was being refereed at the time.

Dr. Croskey is correct in pointing out that these circuits have limitations in their dynamic range. It is to be noted that the circuit under discussion is basically for low-pass applications, whereas the circuit discussed by Dr. Croskey has both low-pass and bandpass behavior. The novelty of the circuit discussed in my note lies in the fact that all the bias resistors are incorporated in the response determining elements of the network. Further, if the optimum bias constraint ($K = 1$) is relaxed, the dc gain may be simply adjusted and the restricted K_{1p} values Dr. Croskey mentions for his circuit do not apply.

If a high-order low-pass filter were to be realized with my circuit, this would be achieved by cascading a series of basic sections of differing Q, ω_n, and if the optimum bias constraint is applied to all sections, the overall structure would be unity gain. Further, the dynamic range problem could be reduced in

[2] Manuscript received January 10, 1977.

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