Short Papers

Performance and Design of Microwave FET Harmonic Generators

MADHU S. GUPTA, RICHARD W. LATON, AND TIMOTHY T. LEE

Abstract—**Experimental measurements of the power gain of a 4- to 8-GHz frequency doubler, employing a single-gate GaAs MESFET device and a microstrip circuit, are reported. The measured performance provides design guidelines, and is explained in terms of FET characteristics. In particular, the multiplication gain is largest when the FET is biased near pinchoff.**

I. Introduction

The nonlinear characteristics of microwave field-effect transistors have recently been used in the design of frequency multipliers by us [1] and by other authors [2], [3]. Both single-gate and dual-gate FET devices have been employed as harmonic generators in the published experiments. The advantages of the FET over a varactor diode in a harmonic generator include better isolation, and a multiplication gain which exceeds unity. This paper reports detailed experimental measurements of the performance of a frequency doubler constructed with a single-gate GaAs microwave MESFET device. The purpose of this work is to 1) experimentally determine the optimum operating conditions (i.e., dc bias and input signal level) which can serve as a guide in design, and 2) qualitatively explain the nature of the operating characteristics of the frequency doubler in terms of the known nonlinear behavior [1] of MESFET devices. The maximum multiplication gain achieved in these experiments is 3 dB, which is higher than that previously reported for single-gate devices.

II. Experimental Arrangement and Results

Fig. 1 shows the frequency doubler circuit, as well as the experimental setup used for measuring the performance of the circuit. The device used is a packaged MSC 88001 microwave GaAs MESFET, mounted in a microstrip circuit in grounded-source configuration. The input and the output frequencies were 4 and 8 GHz, respectively. The input and output ports of the FET are matched and tuned at their respective frequencies by microstrip stubs; in addition, external coaxial stub tuners were also used to optimize the doubler performance by varying the impedances presented to the device at various harmonic frequencies. All the components used in the circuit are designed for use up to X-band (12.4 GHz), which includes both the input and the output frequencies as well as the third harmonic; the impedances at the fourth and higher harmonics are thus dependent on the tuners and the out-of-band response of the components like bias tees. The output circuit also filters out the undesired harmonics, thus improving the spectral purity of the output.

The principal performance parameter of interest in these experiments was the multiplication gain, defined as the ratio of the second harmonic power output to the fundamental frequency power input. Many other parameters of interest, such as the bandwidth and the spectral purity of the output, are very strongly dependent on the circuit and are not determined by the inherent characteristics of the FET device used. The present experiments attempted to establish the dependence of the gain on the device, independent of the tuning circuit, by optimizing the circuit for maximum gain; all gain values reported below are measured under such optimized conditions.

The measured power gain of the frequency doubler is plotted in Figs. 2–4 as a function of the operating conditions. Fig. 2 shows the variation of gain with the gate-to-source dc bias voltage V_G of the FET, for different constant values of the drain-to-source dc bias voltage V_D, at a fixed value of input RF power level $P_{in} = 11$ dBm. Fig. 3 shows the variation of gain with V_D for some constant V_G values, also for the same P_{in}. Finally, Fig. 4 shows the gain variation with P_{in} for two different values of V_G and at $V_D = 4$ V. The conclusions that can be drawn from these plots, and the justification of the nature of observed variations in terms of the device behavior, are discussed in the following.

III. Interpretation of Results in Terms of FET Model

The experimental results reported can be qualitatively understood in terms of the known nonlinear characteristics of microwave MESFET's. One approximate and convenient description of the device characteristics is in the form of a quasi-static equivalent circuit [1]. Briefly, this circuit should include 1) a bias-dependent input (gate-to-source) capacitance, and 2) an output (drain-to-source) current source, controlled by the input and output voltages as indicated by the FET dc characteristics. In particular, the controlled current at the output becomes independent of the input signal when the input voltage either 1) causes forward conduction in the input junction, or 2) reverse biases the junction beyond pinchoff. This simplified model of device behavior explains the following major features of results in Figs. 2–4.

1) Over the entire useful range of V_G, extending from values for which the gate junction is forward biased to values for which it is reverse biased beyond pinchoff, the gain becomes a local maximum at two values of V_G: one near 0 and the other near V_P, the pinchoff voltage of the device, which is approximately 4 V for the devices used. To a first approximation, this can be understood to be due to a one-sided clipping of the input fundamental frequency waveform, either at positive or at negative peaks, which results in the generation of second harmonic component.

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M. S Gupta is with the Department of Information Engineering, University of Illinois at Chicago Circle, Chicago, IL 60680.

R. W. Laton is with Raytheon Company, Missile Systems Division, Bedford, MA 01730.

T. T. Lee is with the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA 02139

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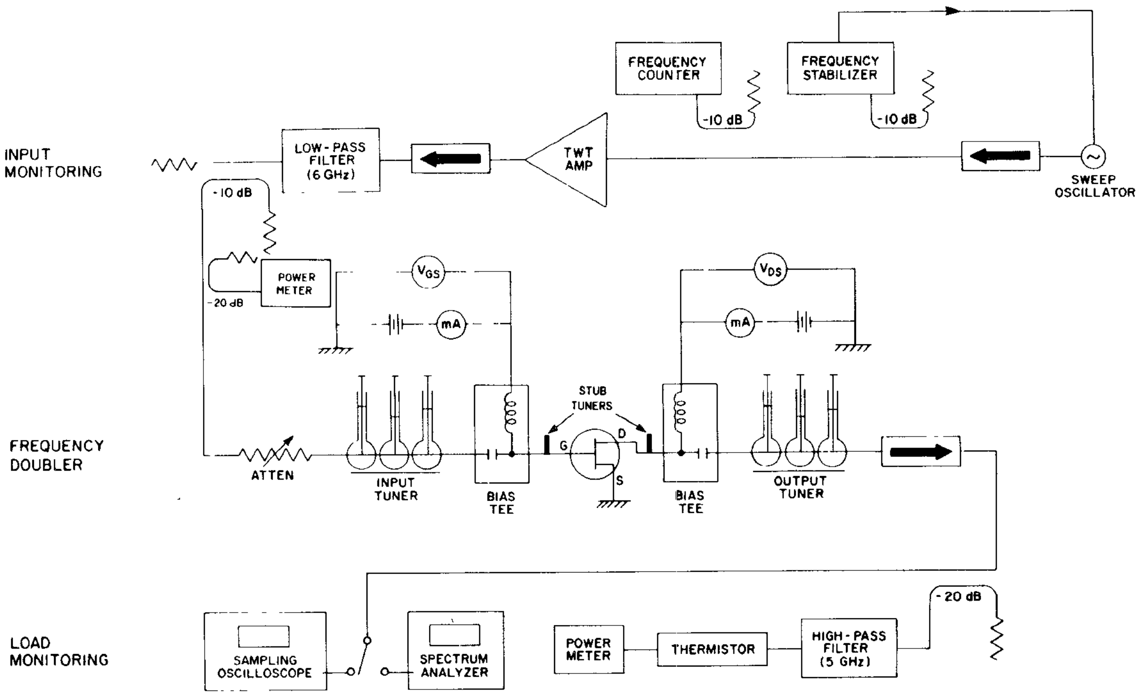

Fig 1. FET frequency doubler circuit and the experimental arrangement for multiplication gain measurement.

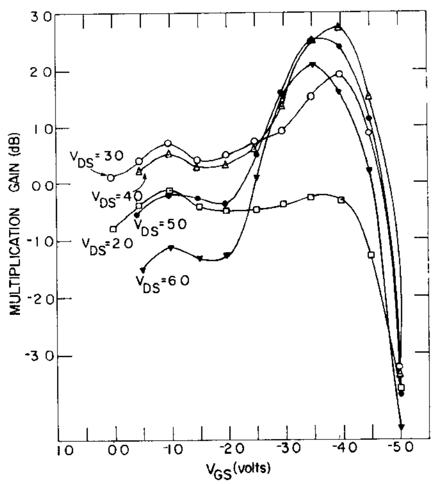

Fig. 2. Multiplication gain of the 4- to 8-GHz frequency doubler as a function of gate and drain dc bias voltages, for a fixed RF input power level of 11 dBm.

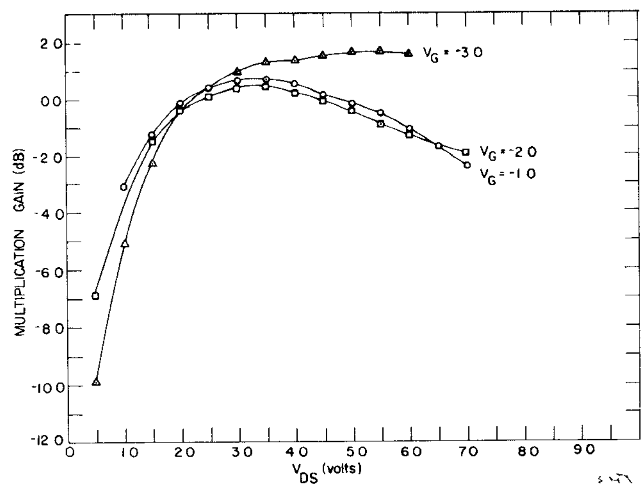

Fig. 3. Multiplication gain variation with drain bias voltage for a fixed input power level of 11 dBm

For a gate voltage in between these two values, the input waveform will be clipped at both positive and negative peaks; the resulting waveform then approaches a square wave, in which the second harmonic content is low. This obviously oversimplified explanation is further supported by the observation that the generation of third harmonic is largest at a gate bias of approximately $V_P/2$. The gain falls rapidly for gate voltages which forward bias the gate junction, or which bias it beyond pinchoff. This can be understood to be due to the small duty cycle for which the transistor is then in the active region.

2) For large values of V_D, the gain maximum is considerably higher for V_G near pinchoff than for V_G near 0. This is partly due to the sharper clipping at pinchoff, but primarily due to the smaller input (i.e., gate-to-source junction) capacitance at pinchoff, so that the same input power results in a larger voltage swing at the input, and therefore a larger drain current swing at the output.

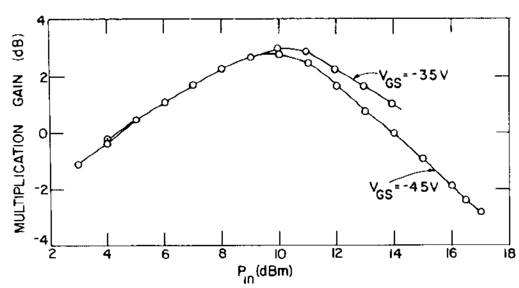

Fig. 4. Multiplication gain of the frequency doubler as a function of the input RF power level for a fixed drain voltage of 4 V.

3) Near its maximum, the multiplication gain is a sensitive function of V_G, but is relatively insensitive to V_D, provided that V_D is large (above 3 V in the present case); when V_D becomes

smaller, the gain drops. This behavior is to be expected on the basis of the FET drain characteristics; the drain current is independent of V_D when V_D is large, and drops to lower values when V_D is small.

4) The power gain of the frequency doubler increases with increasing input power level at small values of P_{in}, reaches a maximum (about 3 dB at 10-mW input in the present case), and then decreases for further increase in P_{in}. The gain expansion at low power levels can be understood from the fact that the device is nearly linear for small signals; the nonlinearity, and hence the harmonic generation, becomes significant only as the signal level becomes large. For very large signals, the output of the device is saturated so that a gain compression occurs.

IV. Conclusions

The multiplication gain of the FET frequency doubler is strongly dependent upon the choice of dc bias voltages. The gain can be maximized by selecting a gate-to-source voltage near pinchoff, and a drain-to-source voltage of approximately the same magnitude. When the bias has been thus optimized, the multiplication gain shows a maximum with respect to the input signal power level.

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On the Design of Transitions Between a Metal and Inverted Strip Dielectric Waveguide for Millimeter Waves

S. BHOOSHAN AND R. MITTRA

***Abstract*—The results of a study of three types of transitions between the rectangular metal waveguide and the inverted strip guide are reported. Reflected power measurements from each type of transition and insertion-loss measurements for configurations involving the three transitions have also been carried out. The procedure of determining the optimum parameters for the transition is quite general, and has the potential for being extended to other dielectric structures.**

I. Introduction

The need for an efficient transition between dielectric and metal waveguides at millimeter-wave frequencies has been recently recognized. The literature on open dielectric structures shows that almost no details of a study of dielectric–metal waveguide transition exist. However, the transitions used to study the effects of such structures could be the basis for investigation [1]. The chief difficulty encountered when studying such transitions is that the wave must pass from an open-waveguiding structure to a closed one, and vice versa, with the field configuration undergoing a complete metamorphosis through the transition region. In this paper, we report the results of an experimental study of several transitions on the basis of the reflected power and insertion loss for these transitions. The dielectric guide used was the homogeneous inverted strip guide, whose cross section is shown in Fig. 1.

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The authors are with the Coordinated Science Laboratory, Electrical Engineering Department, University of Illinois at Urbana-Champaign, Urbana, IL 61801.

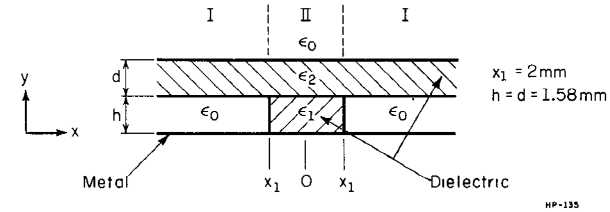

Fig. 1. Cross section of inverted strip guide with typical dimensions.

II. Details of the Study

Two types of transitions were studied: 1) a direct metal to dielectric guide transition, depicted in Fig. 2, and henceforth called transition T-1; and 2) horn-type transitions shown in Figs. 3 and 4, henceforth labeled T-2A and T-2B, respectively.

The study is divided into two parts: a) reflected power measurements from the transition; and b) insertion-loss measurements for a length of dielectric guide introduced between two rectangular metal waveguides which serve as the input and output ports.

A. Reflected Power Measurements

The reflected power measurements for the transition between the metal and dielectric guides were conducted using a length of guide with the transition at its input port. A typical experimental setup consisted of a Y-junction circulator, whose three ports were connected to an RF source, the transition under test, and a power-measuring device. The power from the RF source was incident on the transition, and the power reflected from the same was measured to determine the reflection characteristics. The metal waveguide at the output port of the test setup was terminated by a matched load.

On the basis of these experiments, it was found that the reflection phenomenon in the transition occurs chiefly at two points: (i) at the junction of the metal waveguide and the lower dielectric strip; and (ii) between the lower strip and the top plate of the homogeneous inverted strip guide. The first type of reflection loss can be minimized by inserting an optimum length of taper of the lower strip into the metal waveguide, such that the lower strip is closely matched to the metal guide. The results of the experiments for the determination of the optimum length have been tabulated in Table I, where l_L^* is equal to the optimum value of the inserted length l_L, as shown in Fig. 2. In these measurements, the reflected power was at least 8 dB down as compared to the incident power.

Minimization of the second type of reflection loss can be achieved by using a horn-type feed, as in transitions T-2A and T-2B. Here the tapered top plate was inserted into the horn and the length inserted was adjusted to an optimum value, such that a minimum insertion loss was obtained. A horn-type feed was also instrumental in decreasing considerably the power radiated at the junction by about $\frac{1}{2}$ dB.