A Current-Excited Large-Signal Analysis of IMPATT Devices and Its Circuit Implications

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Abstract—**A large-signal analysis of a Read-type IMPATT diode is carried out with a sinusoidal current as the excitation. The results are compared with analyses that assume a sinusoidal voltage excitation. The large-signal impedance of the diode with current excitation is expressed in closed form. The circuit implications of choosing voltage or current as the excitation are discussed.**

INTRODUCTION

LARGE-SIGNAL analyses of IMPATT diodes and other negative-resistance devices may be classified into two groups [1]: *self-consistent analyses*, in which the device terminal voltage and current are related to each other not only through equations describing the device model, but also by equations describing the terminal characteristics of the circuit in which the device is imbedded, and *idealized-circuit analyses*, in which either the voltage or the current waveform is assumed in advance and the other is calculated through device equations, implying that there exists some circuit that will support this pair of voltage and current waveforms at its terminals. While there is no restriction on the nature of waveforms that may be chosen as the excitation in idealized-circuit analyses, the difficulty of calculating the device response usually dictates the choice. Typically, the waveform chosen is a sinusoid (*single-frequency analysis*), or the sum of several sinusoids of arbitrary amplitudes and relative phases, but with harmonically related frequencies in order to ensure periodicity (*multifrequency analysis*), although other waveforms, such as rectangular ones [2], also have been used.

The single-frequency analyses are most common because their results (impedance or admittance plane plots as a function of the excitation frequency and amplitude) can be more compactly expressed, easily interpreted, and are in a more generally usable form (compare, for instance, the results obtained for a Read-type IMPATT diode from a single-frequency analysis [3], a multifrequency analysis [4], and a self-consistent analysis [1]).

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There are two methods of carrying out single frequency analyses of IMPATT diodes and other negative-resistance devices. The first is the *voltage-excitation* (VE) method, in which a sinusoidal voltage is assumed to be applied across the device, the current response is calculated and Fourier analyzed, and the device impedance is found using the fundamental component of current. The second method is *current-excitation* (CE), in which a sinusoidal current is assumed to flow through the device, voltage response is calculated, and the device impedance is found from it. The first of these methods has been used almost exclusively in the case of IMPATT diodes. In the small-signal case, it does not matter which approach is used because the voltage and current are both sinusoidal; either method therefore gives the same diode impedance. In a large-signal analysis, the harmonic content of the calculated response may be high, and the impedance calculated by the two methods will not be identical, in general. Some caution is necessary in establishing whether the harmonic content is "high" for the following reasons. When the diode response is experimentally determined by means of a probe [5], single-frequency output may be observed in spite of the presence of strong higher harmonics at the device terminals because the diode package is equivalent to a low-pass LC filter [1] that reduces the high-frequency fields outside the diode package. Further, the fact that the current response of the device to a sinusoidal voltage appears almost sinusoidal may be misleading since the largest component of the current is a capacitive component that may well be sinusoidal. The total terminal current of an IMPATT diode (i.e., the external current) is given by [3]

$$I(t) = C_d \frac{d(-V)}{dt} + I_e(t)$$

where C_d is the depletion region capacitance of the diode, V is the ac terminal voltage,[1] and I_e is the terminal current induced by the transport of carriers through the diode (see Fig. 1). For a sinusoidal voltage excitation, the first term is sinusoidal, while the second is usually far from sinusoidal for large signals. As the negative conductance of the device stems from the conductive component of the current, the second term is of primary importance.

[1] The minus sign before V in this and subsequent equations appears because of the sign convention chosen in [3].

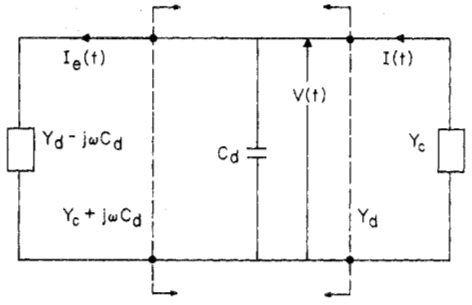

Fig. 1. Terminal voltage and current for an IMPATT diode showing the separation of the depletion region capacitance C_d from the diode admittance Y_d. Y_c is the circuit admittance including the diode package.

When the harmonic content of the response is high, it becomes necessary to specify the assumed harmonic terminations (i.e., the impedance of the circuit at harmonic frequencies) with the results of the large-signal analysis. The assumption concerning the harmonic terminations is implied in the method of the large-signal analysis. The results of several large-signal analyses by the VE method are already available in the literature. The purpose of this paper is to present a large-signal single-frequency analysis with current excitation. The results of the two analyses are compared, and the differences are explained. The circuit implications of the two methods of analysis are then discussed.

Large-Signal Analysis of IMPATT Diodes with Current Excitation

The primary purpose of this analysis is the comparison of the calculated diode impedance using the CE method with that obtained using the VE method. For simplicity, the diode model and the set of assumptions to be made here are so chosen that the analysis remains algebraically tractable. More exact analyses, of course, can be carried out numerically. To avoid duplication, the description of assumptions made concerning the diode and the derivation of the carrier transport equations are omitted. The following equations relating $V(t)$, the ac component of the terminal voltage, and the total (ac plus dc) terminal current $I(t)$ are directly adopted from [3].

$$I(t) = -C_d \frac{dV}{dt} + I_e(t) \tag{1}$$

$$I_c(t) = \frac{1}{\tau_d} \int_{t-\tau_d}^{t} I_c(t')dt' \tag{2}$$

$$\frac{dI_c(t)}{dt} = \frac{2m}{\tau_a E_c} I_c(t) E_a(t) \tag{3}$$

and

$$E_a(t) = E_b - \frac{V(t)}{l_d} - \frac{1}{\epsilon \tau_d A_r} \cdot \int_{t-\tau_d}^{t} (\tau_d - t + t') I_c(t')dt' \tag{4}$$

where the following nomenclature is used.

$I_c(t)$	Carrier current in the avalanche region.
m	$= E_c \alpha'(E_c)/\alpha(E_c)$.
α	Ionization rate for carriers.
E_c	Critical breakdown field so that $\alpha(E_c) = 1/l_a$.
l_d, l_a	Drift region and avalanche region lengths.
τ_d, τ_a	Corresponding transit times.
A_r	Cross-sectional area of the diode.
ϵ	Permittivity of the semiconductor material.
$E(t)$	Total (ac plus dc) electric field strength in the avalanche region.
$E_a(t)$	$= E(t) - E_c$.
E_b	A constant.

The prime denotes differentiation with respect to the electric field, and the assumption $\tau_a/\tau_d \ll 1$ has been made. From (1), the diode admittance (including the depletion region capacitance C_d) at the oscillation frequency ω is given in terms of the fundamental frequency components of current and voltage by

$$Y_d = j\omega C_d - \frac{I_{e,1}(\omega)}{V_1(\omega)} . \tag{5}$$

The set of (2), (3), and (4) has been solved analytically for $I_e(t)$ assuming $V(t) = -V \sin \omega t$, with the additional assumption of a small transit angle [3]. Presently, it will be solved for $V(t)$ assuming[2]

$$I_e(t) = I_{dc} + I_{RF} \sin \omega t. \tag{6}$$

The small transit-angle assumption is unnecessary in the CE method of analysis, as the equations can be solved analytically without it as follows. Substitution of (6) into (2) gives

$$I_c(t) = I_{dc} + A_c \sin \omega \left(t + \frac{\tau_d}{2} \right) \tag{7}$$

where

$$A_c = I_{RF} \frac{(\omega \tau_d/2)}{\sin (\omega \tau_d/2)} . \tag{8}$$

With this, the solution of (3) and (4) for $V(t)$ gives

$$V(t) = \frac{A_c l_d}{\epsilon \omega A_r} \cos \omega \left(t + \frac{\tau_d}{2} \right) - \frac{2 A_c l_d \sin (\omega \tau_d/2)}{\omega^2 \tau_d \epsilon A_r} \cos \omega t - \frac{\tau_a E_c l_d}{2m} \frac{A_c \omega \cos \omega \left(t + \frac{\tau_d}{2} \right)}{I_{dc} + A_c \sin \omega \left(t + \frac{\tau_d}{2} \right)} \tag{9}$$

where the dc equations have been satisfied by setting the constant

$$E_b = \frac{\tau_d I_{dc}}{2 \epsilon A_r} . \tag{10}$$

[2] $I_e(t)$ can be considered as the "terminal" current if C_d is taken to be a part of the passive circuit (see Fig. 1).

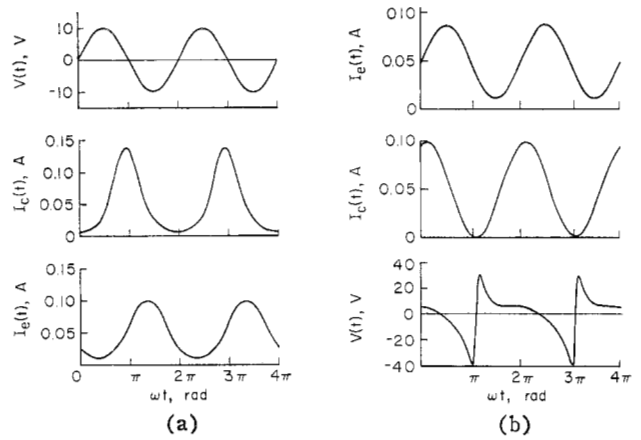

Fig. 2. Comparison of voltage and current waveforms in the (a) VE and (b) CE single-frequency large-signal analyses.

The periodic waveforms of $I_e(t)$, $I_c(t)$, and $V(t)$ given by (6), (7), and (9) are plotted in Fig. 2(b) for a typical set of parameters. For the same diode structure and operating point, the waveforms obtainable from the VE method of analysis are included in Fig. 2(a) for comparison.

The fundamental frequency component of the terminal voltage $V(t)$ found by a Fourier analysis of (9) is

$$V_1(t) = \frac{A_o l_d}{\epsilon\omega A_r}\cos\omega\left(t+\frac{\tau_d}{2}\right) - \frac{2A_o l_d \sin(\omega\tau_d/2)}{\omega^2\tau_d\epsilon A}\cos\omega t - \frac{\tau_1 E_c l_d \omega}{mA_o}\cdot(I_{dc} - \sqrt{I_{dc}^2 - A_o^2})\cos\omega\left(t+\frac{\tau_d}{2}\right). \quad (11)$$

After $I_e(t)$ and $V_1(t)$ in (6) and (11) are represented as phasors and substituted into (5), the diode admittance is found to be

$$Y_d = j\omega C_d + \frac{j\omega C_d A_o I_{RF}\exp(-j\omega\tau_d/2)}{A_o^2 - A_o^2\dfrac{\sin(\omega\tau_d/2)}{(\omega\tau_d/2)}\exp(-j\omega\tau_d/2) - 2I_{dc}\dfrac{\omega^2}{\omega_a^2}(I_{dc} - \sqrt{I_{dc}^2 - A_0^2})} \quad (12)$$

where ω_a is the avalanche frequency defined by

$$\omega_a^2 = \frac{2mI_{dc}}{\epsilon A_r \tau_a E_c}. \quad (13)$$

In the small-signal limit, the admittance becomes

$$Y_{d,ss} = j\omega C_d + j\omega C_d\frac{1-\exp(-j\omega\tau_d)}{\exp(-j\omega\tau_d) - 1 + j\omega\tau_d\left(1-\dfrac{\omega^2}{\omega_a^2}\right)}. \quad (14)$$

The large-signal admittance given by (12) is plotted in Fig. 3(a) as a function of frequency $\omega/2\pi$ and amplitude A_o of the carrier current $I_c(t)$ [which is related to the amplitude of $I_e(t)$ by (8)]. The actual terminal current $I(t)$, which is nonsinusoidal, also can be found by the substitution of (6) and (9) into (1). The admittance plane plot of Fig. 3(a) is redrawn in Fig. 3(b) as a function of I_1, the amplitude of the fundamental frequency component of $I(t)$.

For the purpose of direct comparison, the diode admittance has been calculated by the VE method[3] and the CE method and plotted in Fig. 4 for a fixed value of V_1, the amplitude of the fundamental frequency component of terminal voltage, and for the same device parameters and bias current density. It is clear from Fig. 4 that a single device at one operating point (bias current density, voltage level, and frequency) will have different admittance values depending upon the assumptions made in the method of analysis. This is to be expected because the device is a nonlinear circuit element, and its admittance depends upon the nature of the circuit in which it is imbedded. The two methods of large-signal analysis, VE and CE, tacitly assume two different circuits, as discussed in the next section, and hence yield two different diode admittances.

Model of the Passive Oscillator Circuit

With two different methods resulting in two different impedances, it is necessary to establish the conditions of applicability of the two methods and results. It is well established both theoretically [4], [6] and experimentally [7] that the performance (and impedance) of the diode is influenced by the value of the circuit impedance presented to it at harmonic frequencies. The difference between the VE and CE analyses lies in the different harmonic-frequency circuit impedances that have been tacitly assumed. In the VE analysis, the sinusoidal voltage across the circuit is accompanied by a current that contains harmonics with finite amplitudes. The method therefore should be used for determining diode impedance when the harmonic frequencies are terminated essentially by a short circuit. Similarly, the results of the CE method of analysis are valid when the harmonic frequency terminations are, in effect, open circuits.

There are many situations in which it is essential to have a model for the external circuit of an avalanche diode and other negative-resistance device oscillators. The most straightforward method of modeling is by means of lumped or distributed equivalent networks representing the diode package and cavity. This leads to a broad-band characterization of the circuit [1]. However, for many analytical purposes, such a model is too complicated because it does not ensure single-frequency operation of the nonlinear device, and because its impedance is a complicated function of frequency.

[3] A numerical solution of (2), (3), and (4) as described elsewhere [4] was used; a complete admittance plane plot for this diode and current density is given in [1, fig. 7].

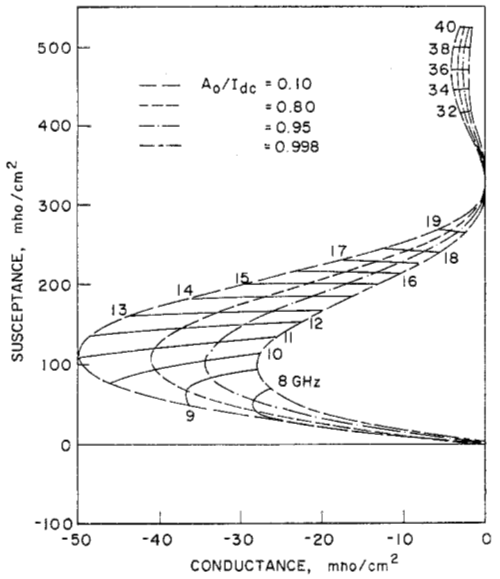

Fig. 3. Admittance plane plot for the Read-type silicon IMPATT diode. (a) As a function of A_0. (b) As a function of I_1. (Avalanche region length = 1 μm, total depletion region length = 5 μm, and bias current density = 500 A/cm^2.)

For these reasons, the circuit commonly has been represented by a lumped *RLC* series, or a parallel resonant network with frequency-independent elements whose impedance is therefore a simple function of frequency. It is important to recognize that the choice of either a series or a parallel resonant network cannot be made arbitrarily; it already has been made in carrying out the large-signal analysis, and once the device impedance has been calculated in one way, there is only one circuit model that may be used with it. In the VE analysis, the circuit impedance should be zero at harmonic frequencies, a condition approached by the parallel resonant circuit, while for the CE type of analysis, the circuit impedance should be infinite at harmonic frequencies, implying that a series resonant circuit is

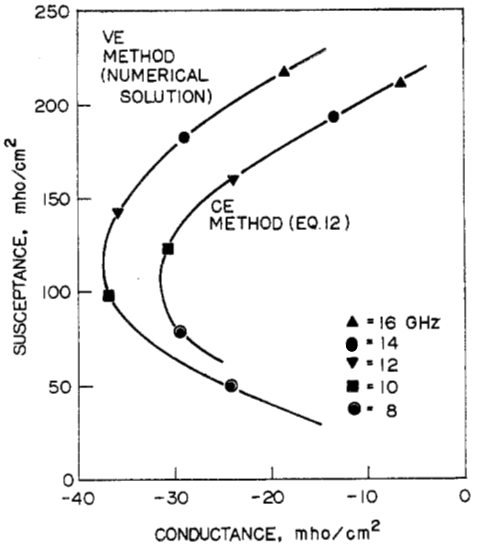

Fig. 4. Comparison of the admittances of the IMPATT diode of Fig. 3 obtained using VE and CE analyses at a dc bias of 500 A/cm^2 and 10-V amplitude at the fundamental frequency.

necessary.[4] These restrictions on the choice of a circuit model are applicable only when the circuit behavior at harmonic frequencies is of concern; when the behavior of the circuit impedance as a function of frequency in the neighborhood of the oscillation frequency alone is of interest, as, for example, in injection locking and noise studies [8], no restrictions are implied, and the choice of a circuit model should be consistent with the stability requirements [8].

In the analysis presented, the current $I_e(t)$ rather than $I(t)$ was taken to be sinusoidal. Therefore, its results are applicable when the admittance of the passive circuit, including the depletion region capacitance, $Y_c+j\omega C_d$, is zero at harmonics of the oscillation frequency, i.e., the circuit admittance Y_c is inductive (see Fig. 1).

Results

The following conclusions may be drawn from Fig. 4.

1) The frequency of maximum negative conductance is lower in the CE analysis than in the VE analysis. This implies that the optimum frequency of operation of a diode is lower when the harmonic voltages are terminated in a high impedance than when they are short circuited. This result can be understood from Fig. 2(b). The phase relationships of harmonic voltages in $V(t)$ are such that the total voltage $V(t)$ becomes small shortly after the avalanche buildup starts. As a result, the injected current $I_e(t)$ increases slowly (sinusoidally instead of almost exponentially) when approaching its maximum value. Consequently, the avalanching phase delay [i.e., the phase shift of $I_e(t)$ with respect to $V_1(t)$] is larger in the CE analysis than in the VE analysis. A

[4] This condition is independent of and unrelated to the well-known stability requirement that "instantaneous" negative resistances with *N*-type and *S*-type *I-V* characteristics only can be connected with parallel and series resonant networks, respectively [9].

smaller transit-time delay is therefore needed for maximum negative conductance. Hence it occurs at a lower frequency.

2) At large signals, a larger negative conductance (and hence power output) is available with the VE analysis than with the CE analysis at all frequencies. This also can be explained by Fig. 2(b). At large signal levels, the injected current $I_e(t)$ in the VE analysis becomes pulsive, and its fundamental frequency component approaches a peak value of $2I_{dc}$ in the limit of the large signal. In the CE analysis, no harmonics of ω are available in $I_e(t)$ to maximize the fundamental frequency component; the limiting value of the amplitude of the fundamental component is therefore only I_{dc}. The generation of a larger fundamental frequency component of $I_e(t)$ in the VE analysis results in a larger negative conductance.

Conclusions

The large-signal admittance of a Read-type IMPATT diode has been calculated, assuming the induced current waveform to be sinusoidal, and analytical results for this model were obtained. The calculated admittance plane plot has been compared with the results of earlier analyses that assumed a sinusoidal voltage across the diode. The difference lies in the assumption regarding the impedance at harmonic frequencies in the passive oscillator circuit, which is inherent in carrying out the analysis with sinusoidal current and voltage excitations, respectively. The large-signal analysis given here is applicable when the passive circuit together with the depletion region capacitance C_d behave like a series resonant circuit at harmonic frequencies, i.e., they have a large impedance.

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Technology for Monolithic High-Power Integrated Circuits Using Polycrystalline Si for Collector and Isolation Walls

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***Abstract*—The fabrication technology for a high-power monolithic IC improved the breakdown characteristics and the output current capability. The maximum output power increased to 50 W and the supplied voltage of 110 V was realized. Highly doped polycrystalline Si was used as the collector walls and the isolation walls of transistors. Electrical and physical properties of the polycrystalline structure used in the power IC and the fabrication technology are also described.**

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I. Introduction

AN OUTLINE of the fabrication technology for a polycrystalline high-power IC has been reported before [1]. In this paper, the details of the technology, the improved electrical characteristics of the newly developed IC's, and the properties of the polycrystalline Si used in the IC are reported. The polycrystalline Si was used as the collector walls connecting the electrodes to the buried layers, and also as the isolation walls in the IC chips. It was possible to construct a