EE 600 – VLSI Testing

Prof. Ke Huang
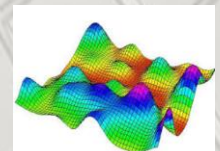### Department of Electrical and Computer Engineering
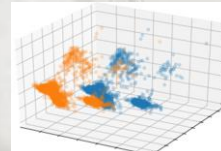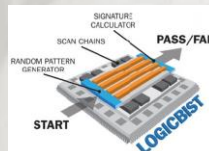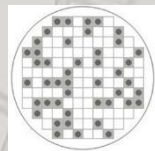### San Diego State University

Course info:

The scale of Integrated Circuits (ICs) has doubled every 18 months following the famous Moore's law. A modern Very-Large-Scale Integration (VLSI) device may consist of hundreds of millions of transistors. This trend brings new challenges in testing those devices in an efficient and cost-effective manner at various stages of manufacturing, as the reduction in transistor feature size increases the probability of defect occurrence during manufacturing. Semiconductor test costs have been growing steadily, which can now amount to 40% of overall product cost. In addition, product quality and yield could drop significantly if these chips are not designed for testability and thoroughly tested.

In this course, we will study a variety of problems encountered in semiconductor testing, as well as new methods being developed to solve these problems at earlier stages of design. Topics covered include design for testability (DFT), scan design/architecture, boundary scan and core-based testing, logic/fault simulation, automatic test pattern generation (ATPG), built-in self-test (BIST), defect and fault diagnosis, memory test, analog/mixed-signal testing, as well as machine learning and data mining applications in VLSI testing.

Instructor Bio:

Prof. Ke Huang received the B.S., M.S. and Ph.D. degrees in Electrical Engineering from the Université Grenoble Alpes, France, in 2006, 2008 and 2011, respectively. He was a Postdoctoral Research Associate at the University of Texas at Dallas from 2012 to 2014. In 2014, he joined the Department of Electrical and Computer Engineering at San Diego State University as an Assistant Professor. His research focuses on machine learning applications in VLSI testing, reliability and security, computer-aided design of integrated circuits, and intelligent vehicles. He has published over 30 journal and conference papers. He served as a Program Committee Member in various IEEE conferences, and as a Guest Editor of Springer Journal of Electronic Testing Theory and Applications (JETTA). He was recipient of the Best Paper Award from the 2015 IEEE VLSI Test Symposium (VTS'15), and recipient of the Best Paper Award from the 2013 Design Automation and Test in Europe (DATE'13) conference.